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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/817,842
Filing Date: March 26, 2001
Appellant(s): GAZDZINSKI, ROBERT F.

Robert F. Gazdzinski
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 25, 2008 appealing from the Office action mailed October 18, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 15-26, 34-41 and 46-55.

Claims 1-14, 27-33 and 42-45 have been canceled.

Claims 15-26, 34-41 and 46-55 are rejected.

Claims 15, 16, 35, 36, 38-41, 46 and 50-53 are being appealed.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.[1]

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,984,875	Brune	11-1999
6,240,312	Alfano et al.	5-2001
6,128,220	Banyai et al.	10-2000
4,061,461	Kratz et al.	8-1977
5,671,247	Souissi et al.	09-1997
6,636,566	Roberts et al.	10-2003
4,862,407	Fette et al.	08-1989
JP 2-82889*	Seiko Epson Corp.	3-1990

PulsON, "Time Modulated Ultra-Wideband for Wireless Applications", 2000Time-Domain Corporation, Time Domain, Rev.2, May 2000, 13 pages (as listed by Applicant in IDS filed 1/12/06)*

[1] The Examiner inquired with an Appeal Specialist regarding the defective nature of the Appeal Brief filed February 25, 2008. It was suggested, and confirmed by a person associated with the Board, that the defects be ignored and that the Examiner proceed with the Examiner's Answer.

*These references were provided in the parent application, which has not been scanned. Since the claims in which these references were used in the rejection are not being appealed by Appellant, these references have not been provided.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

I. REJECTIONS UNDER 35 USC 112, SECOND

Claims 16, 36, 39 and 53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 16, although the description of "optimization" (i.e., selecting a processor core …) appears to be a process step and is given little or no patentable weight with respect to the claimed structure (as discussed below), the term "extension" is vague and indefinite (perhaps "extension instruction" was intended since this is supported by the specification).

As to claim 36, the phrase "having a spreading code that is substantially unique from any other spreading code" is indefinite as to the intended meaning. This would appear to be self-fulfilling (i.e., any particular code is unique from any other one, since they are not the same; unless they are the same, and then they wouldn't be unique).

As to claim 53, comparison of the processor cycles to "that required by a general purpose instruction useful for the same purpose" is indefinite since there is no readily recognizable

reference or standard for "general purpose instruction useful for the same purpose", making the scope of the claim unclear.

II. REJECTIONS UNDER 35 USC 102

Claims 15, 16, 30, 35, 38-41, 46 and 50-53 are rejected under 35 U.S.C. 102(b) as being anticipated by Alfano et al. (U.S. Pat. 6,240,312).

Alfano et al. disclose a probe including at least one sensor (25), a data processor (microcomputer 29), and a communications device (21). Although shown schematically, at least one single semiconductive die or substrate will inherently be incorporated by one or both of the data processor or communications device (e.g., note col.6, lines 1-2). Alfano et al. discloses in column 5, line 66 to col.6, line 12 that the data processor and communications device could be placed on the same die (silicon chip). The data processor inherently includes a core which has a certain power consumption which is "reduced" compared to what it could be and thus optimized (any design for size or power consumption is its own optimal design by nature of being the preferred or chosen design). The data processor also inherently includes an instruction and mathematical operation.

Claims 35, 38, 39, 46, 48 and 50 are rejected under 35 U.S.C. 102(e) as being anticipated by Brune (U.S. Pat. 5,984,875).

Brune disclose a probe including at least one sensor capable of collecting information (col.5, lines 19-27), a data processor adapted to process at least a portion of said information to produce data (col.6, lines 18-31 and col.7, lines 13-14) and a communications device adapted to

transfer at least a portion of said data or information off-probe (col.7, lines 39-60). Use of a small frequency range and FSK techniques (col.6, line 53 to col.7, line 4) will minimize certain interference with other devices (e.g., devices using different frequency ranges), making it "adapted to minimize interference with other communications devices operated proximate said probe" (col.2, lines 42-62). Claims 38 and 39 are product by process claims and are only bound by the structure of the product they imply. The structure mentioned above meet the structural limitations of claims 38 and 39. The components of Brune are formed with IC chips (i.e., microprocessor U1, oscillator U4, etc.) which include dies.

III. REJECTIONS UNDER 35 USC 103

Claims 15-20, 23, 40, 41 and 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brune (U.S. Pat. 5,984,875) in view of Banyai et al. (U.S. Pat. 6,128,220).

Brune disclose a probe including at least one sensor capable of collecting information (col.5, lines 19-27), a data processor adapted to process at least a portion of said information to produce data (col.6, lines 18-31 and col.7, lines 13-14) and a communications device adapted to transfer at least a portion of said data or information off-probe (col.7, lines 39-60). Brune teaches separate IC chips (i.e., microprocessor U1, oscillator U4, etc.). Notwithstanding the fact that the components of Brune are all formed on a single circuit board (note above) and thus, as applicable to claim 40, are designed to be "adapted to be integrated", the components of Brune are not incorporated in one integrated chip which includes a single die. However, the integration of components is "well within the capability of those skilled in the semiconductor design and fabrication arts", as admitted by Applicant (note specification, page 31, lines 3-14). Banyai et al.

teaches that by integrating separate components (e.g., memory) on the same die as a microprocessor, the design "reduces cost and complexity because of the elimination of hardware required and the additional serial protocol required to communicate with an off-chip memory device" (note col.4, lines 24-32). The Examiner takes the position that this concept of integration would, to anyone of ordinary skill, apply to any combinable set of discrete components, including the discrete circuitry of the communications device in Brune. It would have therefore been obvious to one of ordinary skill in the art to have provided the discrete components of Brune on a single semi-conductive die (IC chip die) for the reasons taught by Banyai et al.

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Banyai et al., as set forth above, and further in view of Kratz et al. (U.S. Pat. 4,061,461).

Brune disclose a device as described above which includes a digital data processor but fails to disclose that the processor includes a FFT operation or a butterfly calculation. The Examiner takes the position that digital signal processing for storage and/or transfer commonly uses a FFT operation, and additionally, that butterfly calculations are commonly used in software based FFT calculations. Kratz et al. is just one example of a generic digital data processor which teaches the conventional use of FFT operations (e.g., col.1, lines5-21), including the FFT butterfly (col.76, lines 39+). Since the Brune device is processing and transferring digital data, it would have been obvious to one of ordinary skill in the art to have programmed the processor

with what is known or what is used for this particular purpose, including the FFT butterfly operation.

Claims 24, 25 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Banyai et al., as set forth above, and further in view of Souissi et al. (U.S. Pat. 5,671,247).

Brune discloses a medical device as described above including a conventional RF transmission using conventional FSK or BPSK techniques in the 27 MHz frequency range. It would be obvious to one of ordinary skill in the art to have used a known alternative frequency band, and particularly a free, unlicensed band designated for medical purposes. The ISM bands are one such set of bands. Furthermore, these bands require spread spectrum techniques (note Souissi et al., col.2, lines 13-26) which are particularly well suited for FSK and BPSK transmission techniques, among others. Spread spectrum techniques consists of two schemes: DSSS and FHSS (Souissi et al., col.1, lines 31-38). It would have been obvious to one of ordinary skill in the art to have used any known communication technique for the inherent advantages associated with such technique as an obvious alternative to the communication technique of Brune.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Banyai et al., as set forth above, and further in view of Roberts et al. (U.S. Pat. 6,636,566) or the PulsON article (note item 60 in Applicant's IDS).

Brune discloses a device as described above that wirelessly communicates data. Roberts et al. and the PulsON article both teach use of the TM-UWB technology as being particularly suited for wireless communications for a multitude of reasons (e.g., increased bandwidth, reduced interference, etc.) (note at least col.1, lines 15-32 of Roberts et al. and page 2 of the PulsON article). Because TM-UWB provides an alternative wireless communication technique with many desirable advantages that would be consistent with the application of the Brune device, it would have been obvious to one of ordinary skill in the art to have used such communication technique.

Claims 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Souissi et al.

Brune discloses a medical device as described above including a conventional RF transmission using conventional FSK or BPSK techniques in the 27 MHz frequency range. It would be obvious to one of ordinary skill in the art to have used a known alternative frequency band, and particularly a free, unlicensed band designated for medical purposes. The ISM bands are one such set of bands. Furthermore, these bands require spread spectrum techniques (note col.2, lines 13-26) which are particularly well suited for FSK and BPSK transmission techniques, among others. Spread spectrum techniques consists of two schemes: DSSS and FHSS (col.1, lines 31-38). It would have been obvious to one of ordinary skill in the art to have used any known communication technique for the inherent advantages associated with such technique as an obvious alternative to the communication technique of Brune.

Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Kratz et al.

Brune disclose a device as described above which includes a digital data processor but fails to disclose that the processor includes a FFT operation or a butterfly calculation. The Examiner takes the position that digital signal processing for storage and/or transfer commonly uses a FFT operation, and additionally, that butterfly calculations are commonly used in software based FFT calculations. Kratz et al. is just one example of a generic digital data processor which teaches the conventional use of FFT operations (e.g., col.1, lines5-21), including the FFT butterfly (col.76, lines 39+). Since the Brune device is processing and transferring digital data, it would have been obvious to one of ordinary skill in the art to have programmed the processor with what is known or what is used for this particular purpose, including the FFT butterfly operation.

Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Banyai et al., as set forth above, and further in view of Fette et al. (U.S. Pat. 4,862,407).

Brune discloses the device as described above but fails to disclose the particulars of the signal processing algorithms, such as the use of MAC operations. MAC operations are typically associated with digital signal processors and frequently associated with FFT operations. Fette et al. teaches that MAC operations are an "essential, frequently utilized function within most DSP systems" (col.1, lines 20-22). If not inherent, it would have been obvious to one of ordinary skill in the art to have used MAC operations for processing the signals in the Brune device for the inherent advantages associated with the existence of such operations.

Claims 49 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alfano et al. in view of Seiko Epson Corp. (JP 2-82889).

Alfano et al. discloses RF transmission of the image signal (col.5, lines 66-12) but fails to disclose a compression technique (which would clearly be accommodated by the processor). However, Seiko Epson Corp. (note Constitution section) teaches compressing a video signal before transmission. It would have been obvious to one of ordinary skill to have modified the Alfano et al. device to use such compression technique in order to gain the well known advantages of such technique.

(10) Response to Argument

I. RESPONSE TO SECTION 112(2) REJECTIONS

a) Rejection of Claim 16 under 35 USC 112(2)

The Examiner's rejection of claim 16 under 35 USC 112, second paragraph, concerns the word "extension". How "extension" is intended makes a difference as to the structure that is suggested by the "selecting" process step in this product claim[2]. With reference to the processor core, the specification only mentions "extension instructions" (note page 12, lines 10-20, page

[2] In product-by-process claims, process limitations are given little or no patentable weight. The method of forming the product is not germane to the issue of patentability of the product itself. Further, when the prior art discloses a product which reasonably appears to be either identical with or only slightly different than a product claim in a product-by-process claim, the burden is on the Applicant to present evidence from which the Examiner could reasonably conclude that the claimed product differs in kind from those of the prior art. *In re Brown*, 459 F.2d 531, 173 USPQ 685 (CCPA 1972); *In re Fessman*, 489 F.2d 742, 180 USPQ 324 (CCPA 1974). This burden is NOT discharged solely because the product was derived from a process not known to the prior art. *In re Fessman*, 489 F.2d 742, 180 USPQ 324 (CCPA 1974).

49, line 30 to page 50, line 6, and page 51, lines 16-24). As pointed out by Appellant (Appeal Brief, page 5, lines 22-34), "extension" could refer to "extension hardware" (i.e., logic circuits) which are structural in nature as opposed to instructions which, for all intensive purposes, are program code.

However, no single (or multiple, for that matter) extension instruction or extension hardware is disclosed in the specification that is attributable to satisfying "a target core speed criterion while minimizing gate count". This appears to be a function of the physical design of the processor core in which a *target* core speed and a *minimized* gate count mean nothing structurally unless compared to a reference, and does not necessarily have anything to do with any kind of "extension". In addition, it appears that the word "extension" (as is pertains to an instruction) only has meaning as to an intermediate product since a processor core initially designed for a particular function and a lesser core (i.e., a processor core that lacks that function) that includes an "extension instruction" to provide that particular function is, in the end result, substantially the same thing in function and effect. Thus, the Examiner needed clarification as to the intended meaning of "extension" so as to ascertain the scope of the claim.

b) Rejection of claim 39 under 35 USC 112(2)

With Appellant's explanation appearing on page 6 of the Appeal Brief, which refers back to the discussion of claim 16 and further refers to support in the specification, the Examiner has withdrawn this rejection.

c) Rejection of claim 36 under 35 USC 112(2)

Assuming that "any other spreading code" refers to any other spreading code known to man, it is still indefinite to the Examiner how Appellant can determine whether or not the spreading code intended to be covered by the claim is indeed unique from any other spreading code known to man. Although the Examiner understands the methodology of creating a spreading code described by Appellant on page 6 of the Appeal Brief (see section (c) under 112 (2) Rejections), there is no readily recognizable reference or standard for determining the "uniqueness" of a spreading code and no way the Examiner can determine if prior art spreading codes meet the limitation of being "unique from any other spreading code".

It is noted that Appellant does not discuss the rejection of claim 53 under 35 USC 112(2). It is assumed that Appellant is not appealing this rejection.

II. RESPONSE TO SECTION 102 REJECTIONS

The Examiner is following the order of arguments appearing in the Appeal Brief. It is noted that there is no argument regarding the rejection of claim 15 under 35 USC 102(b) over Alfano. It is assumed that Appellant is not appealing this rejection.

a) Rejection of claim 16 under 35 USC 102(b) over Alfano

As pointed out above in a footnote, product-by-process claims, such as claim 16, are only afforded consideration of the product that the claim suggests. Appellant believes that the

Examiner has ignored "structural" limitations in claim 16. In fact, the Examiner had read the claim with respect to the structure it suggests.

> *16. (Previously presented) The probe of Claim 15, wherein said data processor comprises at least a processor core optimized for power consumption, said optimization comprising selecting a processor core configuration including at least one extension that satisfies a target core speed criterion while minimizing gate count.*

Clearly the claim requires a processor core. Appellant believes that "optimized for power consumption" is a structural limitation that is being ignored by the Examiner. The Examiner contends that it is not being ignored but is being read for only the structure it suggests. First of all, the act of optimizing something must be done with respect to a reference. Designing and using a processor that draws half the current as another processor would be considered as "optimizing power consumption" of the first processor only if the current consumption of the second processor is known as a reference. It is the Examiner's position that the processor selected and used by Alfano et al. is not the most inefficient processor known to man with respect to power consumption. One can always be made more inefficient. In addition, the device of Alfano et al. is designed to run off of a limited power source (battery, col.5, lines 25-27) which would have to be more efficient than some processors that are capable of running off of an unlimited power supply (e.g., commercial electricity). In this way, is it optimized, as desired by Alfano et al., for power consumption. Therefore, without a claimed reference or standard to validate the extent of the act of optimizing, such language as it appears in claim 16, merely an inherent factor in the selection process (of a processor).

Regarding the remaining language in the claim, a processor core is made of logic circuits, registers and instructions. According to Appellant's explanation of 'extensions' (middle of page

5 to page 6 of Appeal Brief), extensions are additional logic circuits, registers and instructions. Whether software or hardware is added to a basic processor core to provide the functions as desired (add extensions) or the core is built from the start to function as desired (no extensions), the end result is a processor core that functions as it is suppose to. Furthermore, the processor will have a speed and gate count that, by inherent nature of designing or selecting, will be in and of itself a target (desired) speed and minimal (as opposed to a maximum) gate count. And as mentioned above with respect to the 35 USC 112 second paragraph rejection of claim 16, the act of minimizing means nothing structurally unless it is compared to a reference.

Therefore, claim 16, as it depends from claim 15, only requires a processor that is designed in a desired fashion and functions in a desired fashion—which includes all processors.

b) Rejection of Claims 39 and 40 under 35 USC 102(e) over Brune

Regarding claim 39, Appellant argues that Brune fails to disclose the structure suggested by claim 39 and points out (in bold) what Appellant believes are the structural limitations (note bottom of page 7 to page 8 of Appeal Brief). Although substantially correct for much of the structure, the Examiner does not agree that the "design" generated for the integrated circuit (lines 4-6 of claim 39) sets forth a structural limitation. This is actually describing an intermediate process step that, in the end, when the design is converted into an integrated circuit (note line 7 of claim 39), produces an integrated circuit that is adapted for processing the sensor data. As set forth above, the "extensions" referred to in the design are merely describing the intermediate process step which results in an integrated circuit with particular functions, e.g., adapted to process sensor data. Turning to Brune, Brune discloses a controller which includes a

microprocessor (i.e., integrated circuit) (col.7, lines 13-15) which, by inherently nature of receiving and operating on the sensor data (col.6, lines 18-42) implements a desired processing on such data. As broadly as claimed, any kind of manipulation of the data would be considered "processing". However, it is noted that such data is combined with other code and put through an error detection and correction algorithm (col.7, lines 32-38) which also encompasses "processing".

Therefore, the Examiner maintains that Brune anticipates the actual structural limitations of claim 39.

Regarding claim 40 (as well as claim 41), the Examiner withdraws this rejection under 35 USC 102(e) over Brune. These claims were properly included in the 35 USC 103(a) rejection over Brune in view of Banyai et al. (note numbered paragraph 8 of the Final Rejection, paper number 20061013) and appear to have been erroneously cited in the 102(e) rejection over Brune.

c) Rejection of Claim 35 under 35 USC 102(b) over Alfano

Regarding claim 35, Appellant argues that the Examiner fails to point out where Alfano teaches minimizing interference with other communication devices of other probes. It is firstly noted that claim 35 recites the multi-probe environment and the other communication devices are recited in an "intended use" sense and are not positively recited as part of the combination. In addition, claim 35 does not require any specific structure (much like most of Appellant's claims) for performing the function of "minimizing interference". Thus, a prior art device that is capable of performing the same function would meet the limitation of being "adapted to minimize interference with other communications devices". It is also noted that the word "minimize" with

respect to interference is given no reference or standard to which it can be compared. Thus, any reduction in interference would constitute "minimizing".

Any radio frequency device inherently has a range (distance of transmission) and thus such range would inherently allow minimal interference in a multi-device environment depending on the distance between the devices. Because of the small power level in the Alfano device, any increase in distance between two of Alfano's probes would reduce interference between the probes. Thus, as broadly as claimed, using two probes in different parts of the body as opposed to in the same part of the body would minimize interference. Alfano's communication device is therefore adapted to be used in a multi-probe environment and adapted to minimize interference with other communications device operated proximate the probe.

Further still, the fact that the Alfano device provides a requisite RF signal that causes it to transmit and receive signals at a particular frequency (15 MHz, col.6, lines 4-8) gives the Alfano device the capability to transmit and receive signals at any frequency (to a certain extent) depending on the requisite RF frequency used. Using a different frequency would, at least to some extent, "minimize interference" with another probe.

Because of the reasons set forth above, the Examiner takes the position that the probe of Alfano is "adapted to minimize interference with other communications devices operated proximate said probe".

d) Rejection of Claims 38-41 under 35 USC 102(b) over Alfano

It appears that Appellant's arguments under this section are only directed at claim 38. Appellant argues that "the Examiner has failed to point out where Alfano teaches or remotely

suggests a data processor is designed so as to specifically consider both die size and power consumption for a given processor speed through at least elimination of gates that would otherwise be present but for said design considerations". What processor isn't when it is designed?

In addition, what "consideration" is given at the time of designing the data processor still produces a final product of a data processor with a particular size, speed and power consumption. The Examiner takes the position that the data processor of Alfano inherently has a particular size, speed and power consumption. Claim 38 clearly does not claim any particular size (which is effected by the number of gates), speed or power consumption that has to be met by the prior art.

Therefore, the Examiner takes the position that Alfano meets the structural limitations of this claim.

e) Rejection of Claim 46 under 35 USC 102(b) over Alfano

As noted by Appellant, the Examiner has based the rejection on the inherent features of a data processor in that Alfano's computer (29) will inherently include and instruction and mathematical operations. The Examiner takes the position that since the computer (29) processes the data from the image sensor (note in Figure 1, data from image sensor 25 goes through computer 29 before sent to communications system 21), certain instructions and mathematical operations inherent to processing data will have to be used. Any instructions or mathematical operations used to convert, store, move and/or prepare for transmitting would be considered "necessary for processing of data".

Except for merely disagreeing with the Examiner, Appellant, throughout prosecution and particularly in section (e) (page 10) of the Appeal Brief, never appears to fulfill the burden of providing evidence that the data processor of Alfano does not possess the characteristics as set forth by the Examiner. In the case that Appellant's disagreement is taken as "proof", the following passages are cited as evidence on the Examiner's behalf:

"A typical computer system includes a central processing unit (or "CPU") which comprises the processor subsystem and a plurality of memory and storage devices (or "memory"). The processor subsystem controls the operation of the computer system by executing a sequence of instructions to perform a series of mathematical operations on data." (underlining added, col. 1, lines 59-65 of Holman, Jr., U.S. Pat. 5,276,832)

"Its processor Pr is characterised essentially in that it comprises but a small number of registers, notably seven registers R.sub.O to R.sub.6 ; of course, it incorporates all the necessary circuits for performing the various processing operations contemplated in a data processing system of this type, i.e., logic operations, mathematical operations, and the like, together with an instruction counter. Obviously, a detailed description of these various circuits is not necessary, since different known arrangements thereof are well known to those conversant with the art" (underlining added,col.4, lines 19-29 of Gernelle, U.S. Pat. 3,974,480).

"In a digital signal processor including an instruction storage means, a program sequence control means responsive to instructions from said instruction storage means for generating control signals, data storage means, address means for addressing data in said data storage means and for generating source and destination addresses for operands and for results of mathematical operations on said operands, data operating means including multiplying means and ALU (arithmetic logic unit) means for performing mathematical operations on data supplied thereto, a plurality of register means for storage of intermediate results of said mathematical operations, and bus means for transfer of signals and data among the plurality of means of said digital signal processor, the improvement comprising:" (underlining added, preamble of claim 23, Uramoto et al., U.S. Pat. 5,204,962).

Therefore, the Examiner takes the position that the processor in Alfano, by nature of being connected to and processing data from the image sensor, will meet the limitations of claim 46.

f) Rejection of Claim 50-53 under 35 USC 102(b) over Alfano

Regarding claim 50 (Appellant lumps 51-53 with 50, but only mentions claim 50), Appellant submits that a similar logic applies as discussed with respect to claim 46. The Examiner resorts to his explanations with respect to claim 46, which appear immediately above.

g) Rejection of claims 39, 40, 52, and 53 under USC 102(b) over Alfano

Regarding claim 39, the Examiner interprets the claim the same way as discussed above in section (c) with respect to the Brune reference.

Regarding claim 40, as pointed out in the rejection, Alfano discloses a sensor capable of generating data, a communications interface (communications device) and a signal processor (processor core), wherein the communications interface and signal processor are incorporated on a single semi-conductive die and the die is located in the probe. These elements just so happen to be the highlighted "structural features" of claim 40 (note page 11, lines 17-27, Appeal Brief). Therefore, the Examiner takes the position that claim 40 is anticipated by Alfano.

Regarding claim 52, again, just as with the words "optimize" and "minimize", claim 52 does not provide any reference or standard such that the term "reduce" would be given much meaning. And again, the act of selecting a processor as claimed essentially results in a processor with a cycle count. It has already been shown, with respect to the discussion of claim 46 in section (e) above, that the processor configuration, including the instructions and operations, are, by nature of being in communication with the other elements of the device (e.g., sensor), particularly adapted to operate with, implement and/or control these elements. Therefore, the Examiner takes the position that the structural elements of claim 52 are met by Alfano.

Claim 53 is really not much different than claims 46 or claim 52 with respect to only structurally defining a processor that is supposed to function as desired. It is noted that claim 53 was rejection under 35 USC 112, second paragraph regarding the phrase "that required by a general purpose instruction useful for the same purpose" (note rejections set forth above). Appellant did not address this and it is assumed that this rejection is not being appealed.

h) Rejection of claim 15 and 40 under 35 USC 102(e) over Brune

It is noted that claim 15 was not rejected under 35 USC 102(e) over Brune in the Final Office Action (October 18, 2006). Therefore, this is not an issue under appeal.

As for claim 40, as noted section (b) above with respect to claims 39 and 40, claims 40 and 41 are withdrawn from the 102(e) rejection over Brune since they are properly rejected in the 103 rejection over Brune in view of Banyai et al.

III. RESPONSE TO SECTION 103 REJECTIONS

a) Rejection of claim 15 under 35 USC 103(a) over Brune in view of Banyai

Appellant argues that circuit board electronics in Brune "teaches away from use in a human being as now rejected in Claim 15, since a board of the type described by Brune simply would not fit within a human intestinal tract (especially along with the remaining components recited in Applicant's claimed invention) unless properly miniaturized".

Although claim 15 recites use in a human as an intended use and sets forth no structure that requires any particular size, the Examiner submits that Appellant's "belief" that the Brune

device would not fit in a human intestinal tract is not supported by evidence. In fact, Brune does not disclose any particular size for the device.

Furthermore, Appellant argues that Brune does not teach or suggest miniaturization. Although no particular size that would evidence miniaturization over any other device is claimed, miniaturization would be an indirect result of integrating semiconductor chips, as taught by Banyai et al. (see rejection). Appellant does not address the Banyai et al. reference or the merits of the rejection of Brune in view of Banyai et al.

Therefore, no convincing evidence or arguments are provided relating to the combination of Brune in view of Banyai et al., the Examiner maintains this rejection.

b) Rejection of claim 36 under 35 USC 103(a) over Brune in view of Soussi

Appellant's arguments regarding this claim are directed to what Brune teaches. The Examiner's rejection previously confirmed what Brune teaches and further sets forth a *prima facie* case of obviousness in view of the teaches of Soussi et al. Since Appellant does not address the merits of this rejection, no comments are necessary from the Examiner.

c) Rejection of claim 51 under 35 USC 103(a) over Brune in view of Banyai

As with claim 15 in section (a) immediately above, Appellant fails to address the merits of the Brune/Banyai et al. combination with respect to claim 51. In addition, claim 51 recites that the data processor (from claim 15) "comprises an integrated circuit design specifically adapted to meet at least one power consumption criterion and at least one die size criterion associated with probe". The data processor of Brune inherently consumes an amount of power

dictated by its design. In addition, the size of the die (in the chip which includes the processor) has a size that is dictated by its design. These parameters are considered sufficient, adequate, and specifically adapted for the probe of Brune by mere nature of Brune's selection of such processor for the disclosed probe. Appellant is not claiming a method and Brune does not have to disclose the steps for or "considerations" given to the design of the processor. All Brune must show is the product suggested by the claims. The Examiner submits that Brune in view of Banyai et al. meets the structural limitation of the claims.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

It is noted that the documents cited in Appellant's Related Proceedings Appendix are not decisions rendered by a court or the Board but only documents from the prosecution of the instant application.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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